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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,646	12/01/2004	Bertrand Johan Edward Hontele	NL 020469	8770

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EXAMINER

AMAYA, CARLOS DAVID

ART UNIT	PAPER NUMBER
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2836

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/516,646	Applicant(s) HONTELE, BERTRAND JOHAN EDWARD	
	Examiner Carlos Amaya	Art Unit 2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/01/2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 December 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>04/11/2005</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the subject matter of claims 2 and 3 regarding the first and second circuit part, the predetermined reference value, and the average value of claim 3 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. This application does not contain an abstract of the disclosure as required by 37 CFR 1.72(b). An abstract on a separate sheet is required.
3. Claim 3 contains subject matter which was not described in the specification. It lacks support for an average value, this average value representing a first signal generated by a first circuit part. Appropriate correction is required.

Claim Objections

4. Claims 2-3 are objected to because there appears to be no support in the specification and the drawings for the first and second circuit parts recited as claimed. With respect to the claims there is no clear description of a reference value as claimed in claim 1 and a desired value of claim 3 generated by the second circuit. Claim 3 is objected to as there is no support for the recited average value.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5 rejected under 35 U.S.C. 102(b) as being anticipated by Fraidlin (US 6,038,142).

With respect to claim 1 Fraidlin discloses a Dc-Dc-converter of the type isolated boost converter comprising (Abstract): input terminals for connection to a DC power source (Figure 1, Column 2 lines 1-4 and lines 53-56), a first circuit branch connecting the input terminals and comprising a series arrangement of an inductive element L (Boost inductor 114) and switching means (Switches 103-106), a control circuit (PWM controller 124) coupled to the switching means for generating a control signal for controlling the conductive state of the switching means, a transformer (Transformer 110) equipped with a primary winding coupled to the switching means, a secondary winding magnetically coupled to the primary winding (Figure 1, the primary windings are coupled to the switches 103-106 with a lump inductance 111, and magnetically coupled to the secondary winding), rectifying means (Diodes 119 and 120 Figure 1 rectify the output of the secondary winding, Column 3 lines 16-17) coupled to the secondary winding, and output terminals coupled to the rectifying means (V_{out} Figure 1 is connected to the rectifier, lines 27-31), characterized in that the control signal has a constant period T (Figure 2 V_{gs} 103,106 and V_{gs} 104, 105 are controlled at a pre-determined value by Controller 124) and in that the converter is further equipped with a current control loop for controlling average value over a period of the control signal of the current through the inductive element L at a constant level (Controller 124 and monitoring circuit 125 control the current through inductive element 114, Column 3 lines 35-36 and lines 41-44).

With respect to claim 2 Fraidlin discloses a Dc-Dc-converter as claimed in claim 1, wherein the Dc-Dc-converter comprises a first circuit part (The first circuit part

generates the first signal consisting of switches 103, 104, 105, and 106 being conductive) for generating a first signal (conducting switches generate a first signal at the output V_{out}) that represents the momentary amplitude of the current through the inductive element L a second circuit part for generating a second signal that represents a predetermined reference value (The reference value is inherently provided and used by the controller to control the switching of transistors which determines the current through the inductor in order to provide a desired output at the transformer), and a comparator (Error amplifier circuit 123) equipped with a first input terminal coupled to the first circuit part, a second input terminal coupled to the second circuit part, and an output terminal coupled to the control circuit (Error amplifier circuit 123 is connected to the controller 124).

With respect to claim 3 Fraidlin discloses a Dc-Dc-converter as claimed in claim 1, wherein the control loop is equipped with a first circuit part for generating a first signal that represents the average value of the current through the inductive element L (Controller 124 controls the operation of the first circuit part by turning the switches 103, 104, 105, and 106 on, Figure 2 shows the behavior of current i_{114} through inductor 114 as the switches are turned on and off), a second circuit part for generating a second signal that represents a desired value of the average value of the current through the inductive element L (Figure 2, shows i_{114} the current through the inductor and how is affected by different switches turning on and off, this switches being controlled by the controller), and a third circuit part coupled with the first circuit part, the second circuit part (The third circuit, error amplifier circuit 123, is magnetically coupled to the first and

second circuit parts) and the control circuit for comparing the first signal and the second signal and for adjusting the duty cycle of the control signal in dependency of the difference between the first and the second signal (Error amplifier 123 compares the first and the second signal values with a reference value, and the controller uses this result to adjust the duty cycle, Figure 1 column 3 lines 32-35).

With respect to claim 4 Dc-Dc-converter according to claim 1, wherein the switching means comprises a first series arrangement (series arrangement compose of switches 104 and 105) of a first switching element (switch 104) and a second switching element (switch 105), and a second series arrangement (second series arrangement composed of switches 103 and 106) shunting the first series arrangement and comprising a third switching element (switch 103) and a fourth switching element (switch 106), and wherein the primary winding is coupled between a common terminal of the first and the second switching element and a common terminal of the third and the fourth switching element (Figure 1).

With respect to claim 5 Fraidlin discloses a Dc-Dc-converter according to claim 4, wherein the control circuit effects a switching cycle comprising a first operational state during a first time interval in which energy is transferred from the DC power source to the inductive element L (Figure 2, time intervals between t1 and t2, Column 3 lines 58-61), a second operational state during a second time interval in which energy is transferred from the DC power source and from the inductive element L to the output terminals by means of a current flowing through the primary winding in a first direction (Figure 2 second state is shown between times t2 , t3, t4 and t5, Column 4 lines 9-11), a

third operational state during a third time interval in which energy is transferred from the DC power source to the inductive element L (Figure 2 after t5 the cycle is repeated and is similar to t1 and t2), a fourth operational state during a fourth time interval in which energy is transferred from the DC power source and from the inductive element L to the output terminals by means of a current flowing through the primary winding in a second direction (This is similar to times t2-t5, but with different switches conducting Column 4 lines 38-40), and wherein the time duration of the first and the second time interval together is equal to a constant predetermined value and also equal to the time duration of the third and fourth time interval together (Figure 2 shows the time duration for the different intervals, from the figure there is a constant value for the first and second time interval, also we see that intervals t1 to t5 would be equal to intervals t1' to t2' not shown in figure 2, corresponding to third and fourth time intervals).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fraidlin (US 6,038,142) in view of Prete (US 5,546,295).

With respect to claim 6 Fraidlin discloses the DC-DC converter as claimed in claim 1. Fraidlin, however, does not disclose that the rectifying means is equipped

with a first series arrangement comprising two diodes and shunting the secondary winding and a second series arrangement comprising two further diodes and shunting the secondary winding. Prete, however, discloses a DC-DC converter with a rectifier means composed of diodes D1 through D4 shunting one end of the secondary winding with the other one (Figure 1, Column 2 lines 62-67).

At time of the invention, it would have been obvious to a person of ordinary skill in the art, to insert two diodes in series as taught by Prete, instead of one, for coupling to the secondary winding to produce a DC output.

The suggestion or motivation for doing so would have been to achieve full wave rectification of the ac voltage present at the secondary winding using a bridge rectifier that uses four diodes instead of two.

9. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fraidlin (US 6,038,142) in view of Streater (US 4,494,180)

With respect to claims 7 Fraidlin discloses the DC-DC converter as claimed in claim 1. However, Fraidlin does not disclose that a solar power converter comprises the DC-DC converter. Streater, however, discloses a DC-DC converter (13) having a solar array (10) as a DC source (Figure 1).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art, to provide the DC-DC converter in a solar power converter that uses as a DC input a solar source.

The suggestion or motivation for doing so would have been to make a solar source more reliable by using a solar DC-DC converter.

With respect to claim 8 Streater in view of Fraidlin discloses the solar power converter as claimed in claim 7, comprising an inverter (14) coupled to the output terminals of the DC-DC converter, Column 2 lines (6-16).

With respect to claim 9 Streater in view of Fraidlin discloses the solar power system comprising a solar panel (10) equipped with photovoltaic cells (Column 2 lines 7-8) and solar power converter (13) of claim 7.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner's supervisor, Brian Sircus who can be reached on (571)272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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